REMARKS

This paper is responsive to an Office Action mailed December 9, 2004. Prior to this amendment, claims 17-48 were pending. After amending claims 17, 18, and 33-36, claims 17-48 remain pending.

Section 3 of the Office Action objects to the drawings as being illegible. Formal drawings were submitted by the Applicant and received at the PTO on April 15, 2002. The drawings were sent in response to a Notice of Incomplete Reply mailed on March 25, 2002. A copy of the return-receipt postcard acknowledging receipt of the drawings is enclosed as Attachment B. In a preliminary amendment, filed by the Applicant on June 27, 2002, Figs. 3 and 6 were replaced with substitute drawing. In the event that these drawings have been misplaced, a complete set of up-to-date drawings is enclosed as Attachment A. Note, these drawings include the replacement Fig. 7a, sent in the previous response, which the Examiner has indicated to be acceptable.

In Section 5 of the Office Action claims 17-48 have been rejected under 35 U.S.C. 112, second paragraph, as incomplete. In response, claims 17, 18, and 33-36 have been amended for greater clarity.

In Section 6 of the Office Action claims 17, 33, and 35 have been rejected as unpatentable under 35 U.S.C. 103(a) with respect to Andresen et al. ("Andresen"; US 3,670,304), in view of Abe et al. ("Abe"; US 5,781,588). The Office Action states that Andresen describes a multi-threshold decision circuit that provides bit estimates, a non-causal circuit to supply a bit value for a current bit estimate in response to a non-causal analysis. The Office Action acknowledges that Andresen does not teach the use of NRZ, but states that it would have been obvious apply Abe's NRZ data format to Andresen, to make the claimed invention obvious. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

The Office Action associates Andresen's Amplitude Sense and Data Gate circuit 20 with the Applicant's multi-threshold circuit. Andresen describes a system that includes a read head 10 to detect an analog signal. A read amplifier 12 hard-limits the received signal, to create a 2-level signal. Andresen mentions that either a high or a low threshold may be used to control AND gate 16 (col. 3, ln. 68-75), and a "zero level" threshold can be used by OR gate 18 (col. 4, ln. 1-17). The two series-connected thresholds are shown as trace "B" (line 22 of Fig. 1) and "C" (line 44 of Fig. 1) in Fig. 2. The composite threshold is shown as signal "D" (Fig. 2) and the output on line 27 (Fig. 1) is shown as signal "E" (Fig. 2). The explanation of Fig. 2 also states that when the amplitude of the digital signal deteriorates, the system reverts back to the analog signal (col. 5. ln. 72 through col. 6, ln 8). Andresen also describes circuitry that is used to create the limiting thresholds. In short, Andresen describes a system that hard-limits analog data using a composite threshold, and uses feedback to control the limiting thresholds.

The hard-limited signal is not the same as the Applicant's bit estimate, because a bit estimate is a preliminary judgment of a symbol value (a "0" or a "1"). Despite the fact that Andresen's hard-limited signal assumes a binary format in most situations, it is not treated as binary data, but merely a step in signal processing. It is not binary data because Andresen makes no attempt to determine symbol values until much later in the process, after signal processing in the Data Detector. The proof of this statement is in that fact that in some circumstances, the input signal is not hard-limited at all, and the analog input signal is passed. This situation occurs in the event of small input signals (col. 5. ln. 72 through col. 6, ln 8). See "E" in Fig. 2, which is line 28 from Fig. 1. Here the signal comes out of limiting after 5 pulses due to a small input signal (see "A").

However, assuming for the sake of argument that the hard-limited signal is a bit estimate, it still does not suggest the claimed invention. Claims 17, 33, and 35 have been amended to more clearly recite that the multi-threshold circuit outputs a plurality of bit estimates for each (input) data. Andresen shows only a single hard-limited signal for each data input (tape track), although there can be up to 9 parallel inputs (tracks), see Fig. 3.

The Office Action also associates comparators 138 and 124 in Figs. 6 and 7, with the Applicant's non-causal circuit. Andresen describes this circuitry as a Data Detector, which is block 28 of Fig. 1. The hard-limited input signal (line 28 in Fig. 1 and "A" in Fig. 6) is the input to the data detector. In the data detector (Fig. 6), the hard-limited signal is converted to narrow pulses and ANDed with the clock pulses. The result is sent to a one-shot 116, to create the data pulse (col. 8, ln. 17-36). Comparator 124 generates the clock pulse ("E" in Fig. 7) from a sawtooth, RC time constant input waveform (col. 8., ln. 37-49). Comparator 138 is used to detect phase error by monitoring waveform "D". If

the "D" pulse is too long, a pulse is generated and sent to the phase error latch, block 26 of Fig. 1 (col. 9, ln. 1-23). Thus, the hard-limited signal, and its derivatives, is compared to various thresholds in the process of generating the ultimate data pulse.

For example, in the process of generating the ultimate data value, input "D" is sent to comparators 138 and 124, and is compared to 2 different, constant level thresholds (R1 and R2). This "D" signal is not being compared to a bit values determined in previous and subsequent clock cycles. The Office Action (page 6) states that "bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles". However, R1 and R2 are merely dc voltages. The constant amplitude voltage levels associated with R1 and R2 can be clearly seen in Fig. 7. Data values that are determined in non-current clock cycles are never introduced into Andresen's data detector 28. There is no non-causal analysis occurring in this circuit.

Abe describes 51 variations of an FSK demodulator (col. 1, ln. 35 through col. 10, ln. 39). A frequency converter converts the received signal to a second frequency lower that the first (received) frequency. The second frequency signal is demodulated to baseband. The baseband signal is compared to a threshold, and the number of threshold crossings is counted. In the embodiment mentioned at col. 23, ln. 42-46 (Fig. 18), the baseband signal is said to be in NRZ format.

With respect to the first *prima facie* requirement to support a case of obviousness, there must be a motivation, either in the references or in the general art, to combine the references. The Office Action states (page 7) that with respect to claims 17 and 33, that it would have been obvious to apply the teaching of Abe (NRZ coding) to Andresen, since Andresen's circuit is designed "to resolve and reproduce digital data and NRZ encoded data is digital data..."

However, this analysis would support a motivation to combine any two references merely on the basis that they both deal with digital data. Surely, the motivation to combine references must be supported with more than simply the use of similar data formats. Besides the fact that Andresen and Abe both use digital data, there appears to be little crossover between a frequency-shift keyed demodulation circuit and a tape drive circuit.

The Office Action also states that "one of ordinary skill in the art would have recognized that the use of non-return to zero NRZ would have provided the opportunity to apply the teachings in the Andresen patent to the specific type of data for which it was designed such as NRZ which is a widely used for of encoding for magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe)." In the cited section (Fig. 37) Abe discusses the improvement of BER through threshold adjustment. Even if an expert were motivated to reduce the numbers of errors in Andresen's system, there appears to be no motivation to use any particular modulation format, such as NRZ, to accomplish this task.

Because of the differences in goals, as well as basic circuitry, it seems unlikely that one skilled in the art would be motivated to combine these references for any purpose. That is, motivation must be based on more than a common use of digital data, or a desire to improve BER. Alternately stated, it is unlikely that a skilled artisan would be motivated to use a tape drive-reading circuit to make modifications to an RF receiver. In summary, the Applicant respectfully submits that a *prima facie* case, supporting a motivation to combine references, has not been made. As support for the Applicant's position, an affidavit has been prepared Dr. Oswin Schreiber, enclosed as Attachment C. A partial list of Dr. Schreiber's publications is enclosed as Attachment D. Dr. Schreiber declares, as an expert in the field, that he finds no motivation to

combine the prior art references. Further, as presented below, Dr. Schreiber finds that even if the references were combined they do not suggest all the elements of the claimed invention.

With respect to the second *prima facie* obviousness requirement, even if the references are combined, there is no reasonable expectation of success. That is, even if an expert where given the Andresen and Abe inventions as a foundation, it is unlikely that they could come up with a circuit that supplies multiple bit estimates for each input data, or a circuit that make a bit value decision based upon a comparison of a current (first) clock cycle bit estimate, with bit values decided in non-current clock cycles.

The combination of references most clearly fails to support the third *prima facie* requirement, as the combination does not teach all the limitations of the invention of claims 17, 33, and 35. First, the claimed invention recites a multi-threshold circuit that provides a plurality of bit estimates for each (input) data. The Applicant submits that neither Andresen nor Abe generate a plurality of bit estimates for each data. It is the Applicant's position that Andresen's hard-limited signal is not a bit estimate, as explained above. Even if Andresen's hard-limited signal could be considered to be a bit estimate, however, Andresen supplies only a single hard-limited signal for each input (tape track). Further, neither Andresen nor Abe describes a circuit that compares a first (current clock cycle) estimate to bit values that were decided in other (non-current) clock cycles. Therefore, neither Andresen nor Abe teach a non-causal circuit.

The combination of references does not explicitly describe the above-mentioned limitations, or suggest any modifications that might make these limitations obvious, and the Applicant requests that the rejections be removed.

Section 7 of the Office Action states that claims 17-48 have been provisionally rejected under the judicially created doctrine of double patenting with respect to copending application 10/077,332 ('332). In response, the Applicant notes that the '332 application was filed after the instant application. Further, the '332 application was filed as a CIP of the instant application. Therefore, a terminal disclaimer seems unnecessary.

It is believed that this application is now in a condition of allowance.

Respectfully submitted,

Date: 2/8/2005

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